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A blog to explore whole VLSI Design, focused on ASIC Design flow, Physical Design, Signoff, Standard cells, Files system in VLSI industry, EDA tools, VLSI Interview guidance, Linux and Scripting, Insight of Semiconductor Industry and many more.

Physical Verification Interview Questions - Team VLSI

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Physical Design (Power planning) Interview Question Part 5

Physical Design (PD) Interview Questions - Floorplanning. 1. What is floorplanning? A. Floor planing is the process of placing Blocks/Macros in the chip/core area, thereby determining the routing areas between them. Floorplan determines the size of die and creates wire tracks for placement of standard cells. ... Congestion in VLSI Physical ...

Physical Design (PD) Interview Questions - VLSI Basics

Physical Verification Interview Questions. What is Physical Verification? What are the Sign checks after generating layout?

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Difference between LVS and DRC? Define LEC? What is meant by Pitch? Differentiate Pitch and Spacing between metal layers? What are the common DRC checks? Discuss about Antenna check?

Physical Verification Interview Questions ~ VLSI Guide

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Below are the sequence of questions asked for a physical design engineer. In which field are you interested? Answer to this question depends on your interest, expertise and to the requirement for which you have been interviewed. Well..the candidate gave answer: Low power design; Can you talk about low power techniques?

Backend (Physical Design) Interview Questions and Answers

250+ Physical Design Engineer Interview Questions and Answers, Question1: Why metal density rules are important? Question2: Why power stripes routed in the top metal layers? Question3: Types of checks that can be done in Prime Time ? Question4: How do you validate your floorplan and what analysis you do during floorplan?

TOP 250+ Physical Design Engineer Interview Questions and ...

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10+ years of industrial ...

Floor Planning and Power Planning Interview Questions

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It checks the design whether it is working properly at specified operating frequency by checking the Timing Constraints predefined by vendor tool are meeting by the all timing paths across design. Here I am sharing very basic level interview questions on Static Timing Analysis. you can find the elaborate explanations in further posts.

Static Timing Analysis (STA) Interview Questions ~ VLSI

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Here are eight VLSI interview questions and answers that potential hiring managers may ask you during an interview to determine if you're the right fit for the role. ... It needs to be mentioned that for design purposes, the hold requirement has to be met.

8 VLSI Questions you must study before your next interview ...

1. explain the project WLAN SOC has following components 2 subsystems (WLAN and Microcontroller Sub systems) Our team was responsible for Microcontroller SS verification Microcontroller Subsystem AHB Fabric (AHB interconnect) Cortex M4 subsystem DMA controller, USB controller Code RAM0/1, Data ...

SOC Interview questions - vlsi

VLSI INTERVIEW QUESTION: Static Timing analysis Kindle Edition by Puneet Mittal (Author) Format: Kindle Edition. 3.2 out of ... Very good for aspirants in ASIC design and physical design

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